IN THE SPECIFICATION

Please replace the paragraph beginning on page 6, line 19 with the following replacement paragraph:

To configure ASIC 200 so that its logic blocks are programmed with the same truth table as in FPGA 5, permanent connections are made in the logic blocks such as by a via mask customization or a metal layer customization process performed during manufacture. Figure 4a illustrates a cross-sectional view of ASIC 200 using a via mask customization process. As is known in the semiconductor arts, components such as multiplexers 310 and 320 may be formed in an active layer 380 of a semiconductor wafer used to form ASIC 200 as seen in Figure 4a. In a separate metal layer 385, traces 340 and 350 carry VCC and VSS, respectively (for illustration clarity, additional layers that would overlay metal layer 385 are not shown). To provide the truth table inputs to multiplexers 310, a set of vias 355 would extend between traces 340 and 350 in metal layer 385 to separate metal layer 390. Traces on metal layer 390 are coupled by other vias 395 to couple the signals to active layer 380. As with the remaining components in ASIC 200, vias 395 would be "hardwired" in that it is just vias 355 that are customized to provide the required truth table. Referring again to Figure 3, potential via locations 305 are shown between each multiplexer 310 input and both traces 340 and 350. In actual practice, only one of these via locations 305 (for each multiplexer input) would actually be occupied by a via depending upon whether the truth table input should be true or false. A single via mask processing step during manufacture may be used to indicate which trace (340 or 350) should be connected to a via 355 ~~350~~. If traces 340 and 350 are not carried on the same metal layer, at least two mask steps would be required, one for each metal layer. LUT 300 also supports a carry-in, carry-out cascade and arithmetic functions through carry-out multiplexer 330 ~~350~~ and XOR gate 360.

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Please replace the paragraph beginning on page 6, line 19 with the following replacement paragraph:

Just as LUT 300 matches the LUT it is intended to model in FPGA 5, routing in ASIC 200 will also match the routing in FPGA 5 ~~FPGA5~~. As with the LUT architecture, the routing configuration will be device-dependent and thus will vary according to the particular programmable logic device being modeled. For example, FPGA 5 may have a buffered-segmented routing structure whose segments span a certain number of logic blocks in either a row or column direction. In such a buffered-segmented routing structure, a certain portion of a segmented routing structure may span two rows or columns and thus be denoted as a segment-2 routing resource. Other portions of a segmented routing structure would span more than 2 rows or columns, depending upon the particular design used for the routing structure. Figure 5 illustrates an exemplary segment-2 routing structure portion 500 for FPGA 5. A 20:1 multiplexer 505 selects from a group of twenty signals to provide an output to be carried on segment-2 routing structure portion 500. Theses signals are carried on four buses denoted as X6, X2, X1, and F/Q. As is known in the art, the selection by multiplexer 505 is controlled by configuration signals. Thus, during operation of FPGA 5, the selection by multiplexer 505 does not change. Also conventional in the art is the use of a buffer 510 to isolate capacitive loading and provide related benefits. Segment-2 routing structure portion 500 spans two columns (of PFUs) such that at each column it fans out to a plurality of outputs. At a first column 520, these outputs are denoted as VX2, ISB, X0, and VX2. At a second column 525, these outputs are denoted as VX2, 2 X6, ISB, X0, 2 HX2, and VX2. To illustrate coupling between segments, a portion of another segment-2 routing portion 590 is shown. Its 20:1 multiplexer 505 selects for one of the HX2 signals from segment-2 routing

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portion 500 to provide the output onto segment-2 routing portion 590. To model this routing in FPGA 5 into that used in ASIC 200, the same routing delay between segments should be incurred. With respect to Figure 5, this routing delay may be denoted as that incurred between inverter 575 and inverter 595.

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